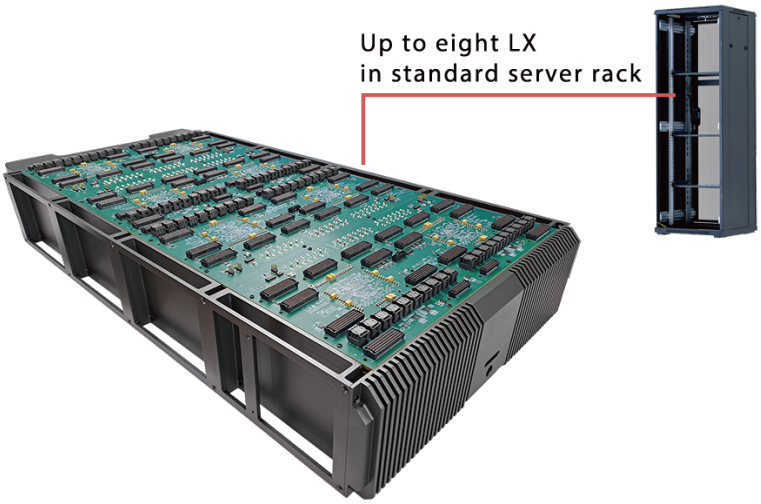
Prodigy™ LX1 Logic Matrix

The Prodigy™ LX1 Logic Matrix is a high-density FPGA prototyping platform architected from the ground up to meet today's needs for both large design scaling and performance. Optimized for space and connectivity, LX1 is designed for multi-system expansion to support bills of ASIC gate capacity. LX1 is the ideal solution to address the ever-increasing complexity AND performance requirements found in large scale SoC designs for applications such as 5G, datacenter, AI/ML, and autonomous driving.

Highlights

- Industry leading density and capacity - up to 1.92billion ASIC gates in single standard server rack
- Hierarchical connectivity to support flexible topology and hyperscale design at prototyping performance
- Highly modular design to simplify deployment, maintenance, and expansion in via standard server racks
- Multi-usages: early software development, full system integration, high performance regression



Features

Large Capacity & Scalability

- LX1 available in 2, 4, 6, or 8 Xilinx VU440 FPGA configuration offering up to
  - 44.32M System Logic Cells
  - 708.8Mb of internal memory
  - 23,040 DSP Slice
- House up to 8 LX1 or 64 FPGAs in single standard server rack
- Interconnect multiple server racks for large scale deployment
- Future upgrade made easy - same physical dimension as LX2

Flexible Topology & Hierarchical Connectivity

- Advanced Clock Management
  - 12 global clock inputs, 3 global clock outputs and 4 global resets
  - Dedicated global control module to synchronize clocks & resets across multiple systems
- Hierarchical Connectivity using 9,984 GPIO & 384 GTH transceivers
  - ShortBridge: high throughput connectivity between neighboring FPGAs
  - SysLink: high throughput cable for local and neighboring system connectivity
  - TransLink: long distance links between FPGAs with SerDes over copper or optical cables

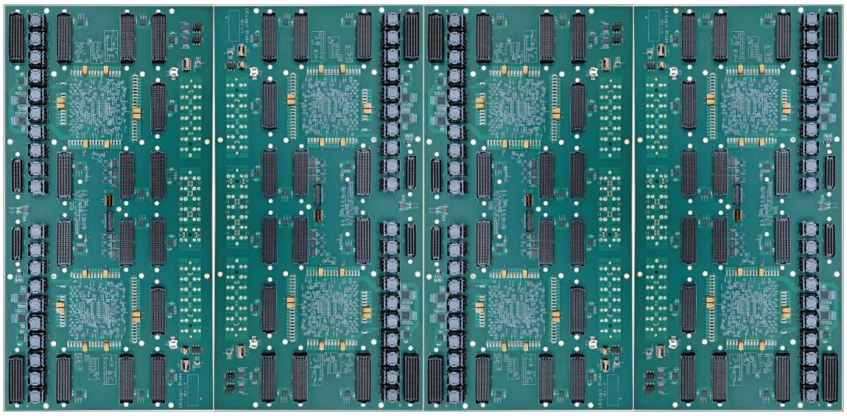
Features

High Reliability

- Redundant hot pluggable power supplies keep the system always online
- Professional air duct & heat pipe design
- Screw-locked high speed I/O connectors

I/O Architecture

- 64 Prodigy Connectors each supports 144 single-ended / 72 LVDS pairs
- I/O voltage can be adjusted to 1.0V ~ 1.8V
- 80 Mini-SAS connectors each supports 4 GTH transceivers and 8 GPIOs
- 8 PGT connectors each supports 8 GTH transceivers and 16 GPIOs



Configuration Table

	LX1-11	LX1-21	LX1-31	LX1-41
FPGA Count	2	4	6	8
System Logic Cells (M)	11.08	22.16	33.24	44.32
Estimated ASIC Gates (M)	60	120	180	240
FPGA Memory (Mb)	177.2	354.4	531.6	708.8
DSP Slices	5760	11520	17280	23040
External User I/Os	2496	4992	7488	9984
GTH Transceivers	96	192	288	384
Prodigy Connectors	16	32	48	64
PGT Connectors	2	4	6	8
Mini-SAS Connectors	20	40	60	80