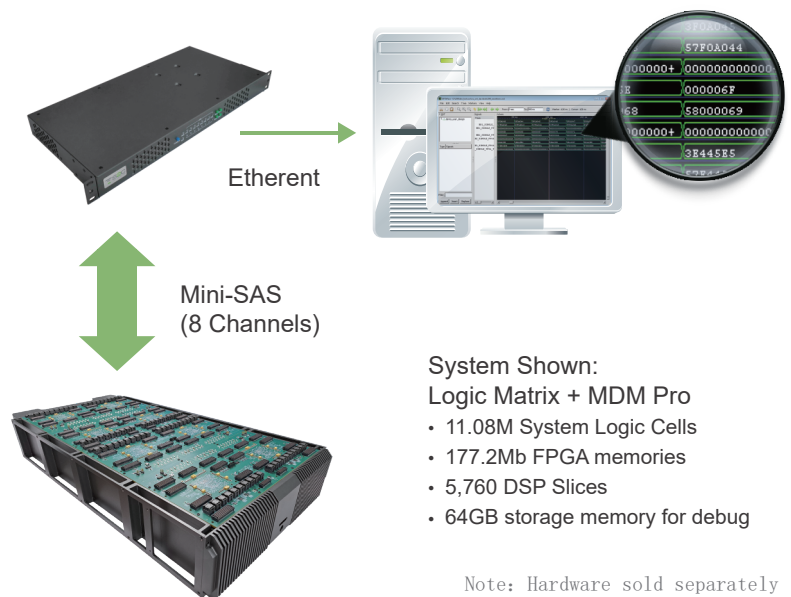# Prodigy™ Multi-Debug Module Pro

Prodigy Multi-Debug Module Pro (MDM Pro™) is an innovative deep trace debugging solution for FPGA prototyping and allows for the concurrent debugging of multiple FPGAs. Prodigy MDM Pro works within the Prodigy Player Pro™ cockpit to go beyond debug set up to specify trigger conditions then debug multiple FPGAs with the help of the dedicated hardware. The MDM Pro hardware enables massive data acquisition and transferring through high speed giga transceivers, and deep tracing of the cause of bugs with the ability to store up to 64GB of waveforms. The MDM Pro captures and stores waveforms continuously removing the need to consume design FPGA memory for debug.

Highlights

- Debug across up to 8 FPGAs simultaneously using a single logic analyzer

- Sampling frequency at speeds up to 125MHz

- Trace up to 2K probes per FPGA and support 8 sample groups

- Easy get the value of any internal DFF/BRAM

- Supports trigger state machine languages to ease the debugging

- Store up to 64GB of waveform data externally

Etherent

Mini-SAS
(8 Channels)

System Shown:
Logic Matrix + MDM Pro
- 11.08M System Logic Cells
- 177.2Mb FPGA memories
- 5,760 DSP Slices
- 64GB storage memory for debug

Note: Hardware sold separately

Features

The MDM Pro supports two usage modes: Compiler mode and IP mode. In IP mode, users can instantiate the debug IP in the DUT directly, no need to run the Player Pro compile time flow. When running the compiler mode, it is embedded in Prodigy Player Pro, the advanced multiple FPGA debug capabilities include:

RTL-level Probing

- The GUI allows you to mark and upload internal signals to the external MDM Pro hardware for easy setting of trigger conditions and signal tracing.

Large Number of Probes Without Re-Compile

- Mark an unlimited number of internal FPGA probes before synthesis

- Trace up to 16K probes per FPGA in 8 groups of 2K probes each without FPGA re-compilation

Integrated In-Circuit Debug Setup

- Set up trigger and trace signals in multiple FPGAs from a single console

- Preserve internal FPGA probes before synthesis

- Probes are distributed to multiple FPGAs automatically based on partition results

Features

Trigger Condition Specification

General Trigger

Users can easily set trigger events and combinational events

- Trigger events support: ==, !=, >=, <=, >, < and counting

- Combinational events support: !, &, |, ^, -> and counting

- Supports up to 8 event trigger blocks. Each block can run comparison, sequencing, occurrence and combination operations

Advanced Trigger

- Up to 8 trigger comparators

- State machines - support up to 16 states

- One, two- and three-way conditional branching

- Four built-in 16-bits counters used to events, implement timers, etc.

- Four built-in flags used for monitoring trigger state machine execution status
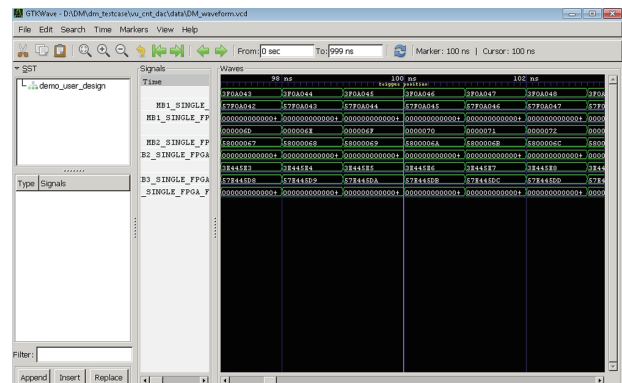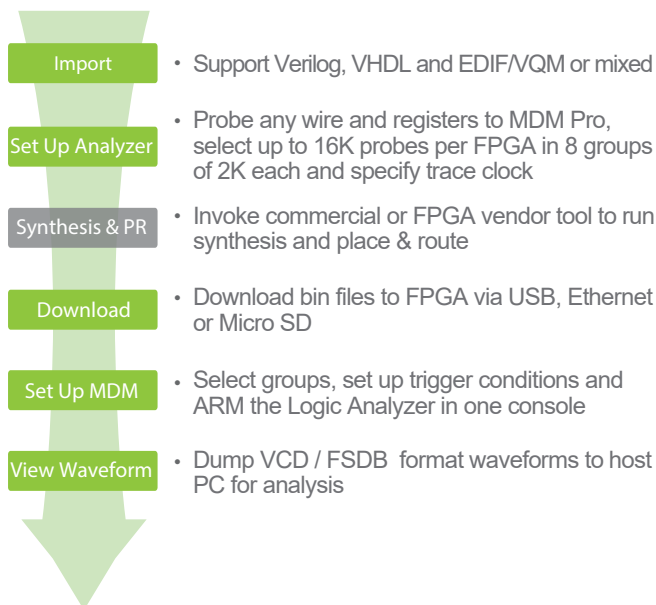
64GB Deep Trace

- Store 64GB of waveforms on external DDR4 memory, minimize the consumption of user FPGA resources

- Transfer captured waveforms to host computer through Gigabit Ethernet

- Capture and store waveforms continuously

Concurrent Debug of Multiple FPGAs

- Debug across multiple FPGAs simultaneously using a single Logic Analyzer

- Easy get the value of any internal DFF / BRAM

- Transmit trigger and trace data from multiple FPGAs to the MDM Pro hardware through high-speed transceivers

- Write the sample data in VCD / FSDB/ FST format for analysis

Integrated with Prototyping Setup Flow

Prodigy MDM Pro works within the Prodigy Player Pro cockpit to go beyond debug set up to specify trigger conditions then debug.

Import	• Support Verilog, VHDL and EDIF/VQM or mixed
Set Up Analyzer	• Probe any wire and registers to MDM Pro, select up to 16K probes per FPGA in 8 groups of 2K each and specify trace clock
Synthesis & PR	• Invoke commercial or FPGA vendor tool to run synthesis and place & route
Download	• Download bin files to FPGA via USB, Ethernet or Micro SD
Set Up MDM	• Select groups, set up trigger conditions and ARM the Logic Analyzer in one console
View Waveform	• Dump VCD / FSDB format waveforms to host PC for analysis

Concurrent Debugging of Multiple FPGAs in one console

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